

Vishay Siliconix

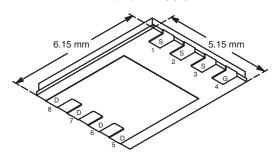
## N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}$ ( $\Omega$ )	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)		
100	0.014 at V <sub>GS</sub> = 10 V	60	47.5 nC		

#### **FEATURES**

- Halogen-free
- TrenchFET® Power MOSFET
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested

#### PowerPAK SO-8

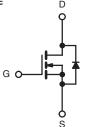


**Bottom View** 

Ordering Information: Si7178DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

#### **APPLICATIONS**

- Primary Side Switch
- POL
- Intermediate Bus Converte-



N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATIN</b>	IGS T <sub>A</sub> = 25 °C,	unless otherwis	se noted		
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	100	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	V	
	T <sub>C</sub> = 25 °C		60		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 70 °C	I <sub>D</sub>	48		
Continuous Brain Current (1) = 100 °C)	T <sub>A</sub> = 25 °C	טי [	14.9 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		11.9 <sup>b, c</sup>	Α	
Pulsed Drain Current		I <sub>DM</sub>	80	^	
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C		60		
	T <sub>A</sub> = 25 °C	I <sub>S</sub>	5.2 <sup>b, c</sup>		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	40		
Single Pulse Avalanche Energy		E <sub>AS</sub>	80	mJ	
	T <sub>C</sub> = 25 °C		104		
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	P <sub>D</sub>	66.5	W	
Maximum Fower Dissipation	T <sub>A</sub> = 25 °C	' b	6.25 <sup>b, c</sup>	VV	
	T <sub>A</sub> = 70 °C		4.0 <sup>b, c</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260	°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	$R_{thJA}$	15	20	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	0.9	1.2	0/11	

#### Notes:

- a. Based on T<sub>C</sub> = 25 °C.
  b. Surface mounted on 1" x 1" FR4 board.
- d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

  e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 54 °C/W.

## **Si7178DP**

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static					L	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 vA		130		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 10		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	2.5		4.5	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$			1	μА
		$V_{DS}$ = 100 V, $V_{GS}$ = 0 V, $T_{J}$ = 55 °C	V, T <sub>J</sub> = 55 °C		10	μ, τ
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	40			Α
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		0.0114	0.014	Ω
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_{D} = 10 \text{ A}$		28		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>			2870		pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		225		
Reverse Transfer Capacitance	C <sub>rss</sub>			91		
Total Gate Charge	$Q_g$			47.5	72	nC
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$		13.2		
Gate-Drain Charge	$Q_{gd}$			12.7		
Gate Resistance	$R_g$	f = 1 MHz	0.3	1.15	2.3	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			18	35	ns ns
Rise Time	t <sub>r</sub>	$V_{DD}$ = 50 V, $R_L$ = 10 $\Omega$		10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 5$ A, $V_{GEN}=10$ V, $R_g=1$ $\Omega$		27	50	
Fall Time	t <sub>f</sub>			10	20	
Turn-On Delay Time	t <sub>d(on)</sub>			21	40	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 50 V, $R_L$ = 10 $\Omega$		10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong$ 5 A, $V_{GEN}$ = 8 V, $R_g$ = 1 $\Omega$		27	50	
Fall Time	t <sub>f</sub>			11	20	
<b>Drain-Source Body Diode Characteristi</b>	cs					
Continuous Source-Drain Diode Current	I <sub>S</sub>	$T_C = 25  ^{\circ}C$			60	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				80	A
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 4 A		0.76	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>			64	100	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	L = 10 A di/dt = 100 A/us T = 25 °C		200	300	nC
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$		51		
Reverse Recovery Rise Time	overy Rise Time t <sub>b</sub>			13		ns

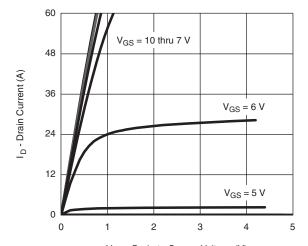
- a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



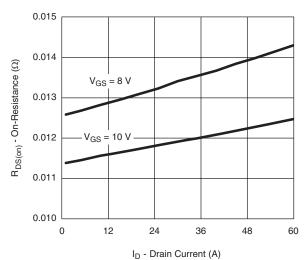
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### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

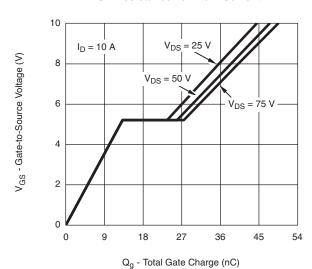


 $V_{\mbox{\scriptsize DS}}$  - Drain-to-Source Voltage (V)

#### **Output Characteristics**

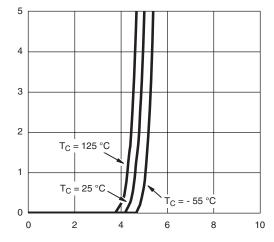


On-Resistance vs. Drain Current



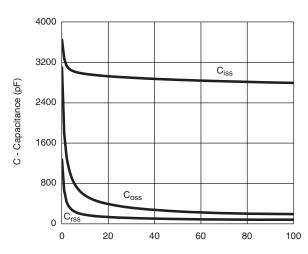
**Gate Charge** 

I<sub>D</sub> - Drain Current (A)



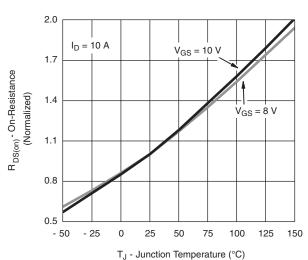
V<sub>GS</sub> - Gate-to-Source Voltage (V)

#### **Transfer Characteristics**



 $V_{\mbox{\footnotesize DS}}$  - Drain-to-Source Voltage (V)

#### Capacitance



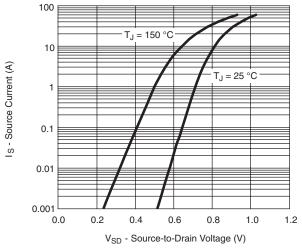
On-Resistance vs. Junction Temperature

## **Si7178DP**

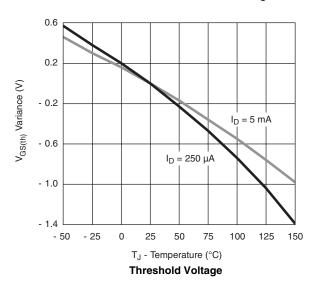
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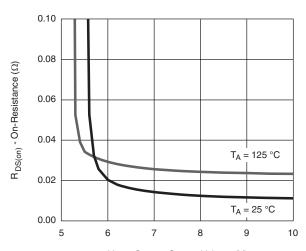
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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

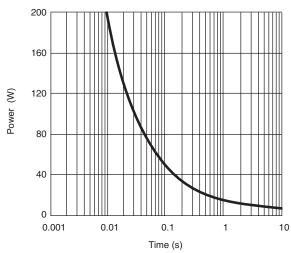


#### Source-Drain Diode Forward Voltage

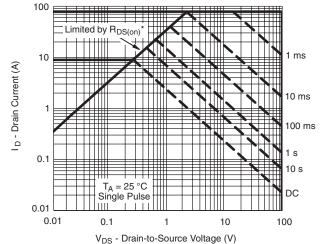




 $\label{eq:VGS} V_{GS} \mbox{ - Gate-to-Source Voltage (V)} \\$  On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



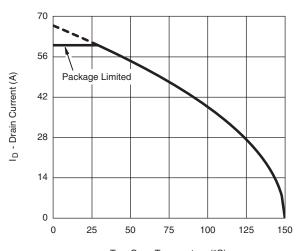
\* V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified

Safe Operating Area, Junction-to-Ambient



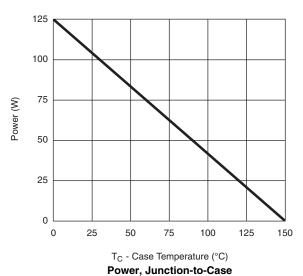
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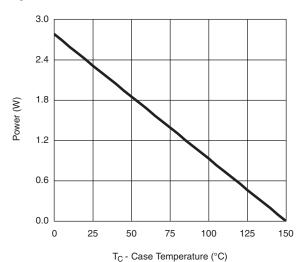
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



 $T_{\mbox{\scriptsize C}}$  - Case Temperature (°C)

#### **Current Derating\***





Power, Junction-to-Ambient

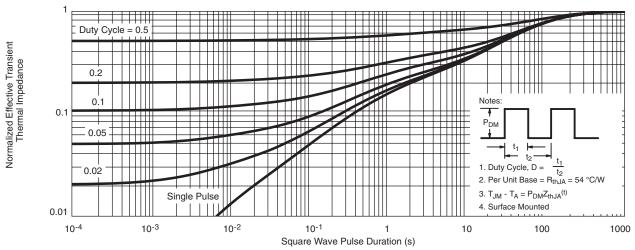
<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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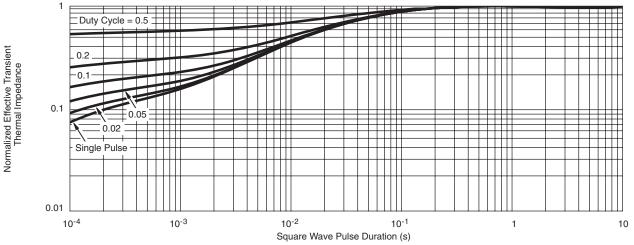
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#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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